KONGU ENGINEERING COLLEGE, PERUNDURAI, ERODE – 638 052
(Autonomous Institution affiliated to Anna University of Technology, Coimbatore)

M.E. DEGREE IN VLSI DESIGN (FULL-TIME)

CURRICULUM
(For the candidates admitted from academic year 2011 – 12 onwards)

SEMESTER - I

Course Code	Course Title	Hours / Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	THEORY							
11VL101	Applied Mathematics for Electronic Engineers	3	1	0	4	50	50	100
11VL102	Advanced Digital System for IC Design	3	1	0	4	50	50	100
11VL103	VLSI Design Techniques	3	0	0	3	50	50	100
11VL104	VLSI Signal Processing	3	1	0	4	50	50	100
11VL105	Device Modeling	3	0	0	3	50	50	100
11VL106	HDL for IC Design	3	0	0	3	50	50	100
	PRACTICAL							
11VL107	Simulation and Synthesis Laboratory	0	0	4	2	100	0	100
				Total	**23**			

CA – Continuous Assessment, ESE – End Semester Examination

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CURRICULUM

(For the candidates admitted from academic year 2011 - 12onwards)

SEMESTER - II

Course Code	Course Title	Hours / Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	THEORY							
11VL201	Analysis and Design of Analog Integrated Circuits	3	0	0	3	50	50	100
11VL202	Application Specific Integrated Circuits	3	0	0	3	50	50	100
11VL203	Testing of VLSI Circuits	3	0	0	3	50	50	100
11VL204	Digital Signal Processing Integrated Circuits	3	0	0	3	50	50	100
	Elective - I	3	0	0	3	50	50	100
	Elective - II	3	0	0	3	50	50	100
	PRACTICAL							
11VL205	Programmable Devices Laboratory	0	0	4	2	100	0	100
11VL206	ASIC Design Laboratory	0	0	4	2	100	0	100
				Total	**22**			

CA – Continuous Assessment, ESE – End Semester Examination

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M.E. DEGREE IN VLSI DESIGN (FULL-TIME)

CURRICULUM
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SEMESTER - III

Course Code	Course Title	Hours / Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	THEORY							
	Elective - III	3	0	0	3	50	50	100
	Elective – IV	3	0	0	3	50	50	100
	Elective - V	3	0	0	3	50	50	100
	PRACTICAL							
11VL301	Project Work – Phase- I	0	0	12	6	50	50	100
				Total	**15**			

CA – Continuous Assessment, ESE – End Semester Examination

SEMESTER - IV

Course Code	Course Title	Hours / Week			Credit	Maximum Marks		
		L	T	P		CA	ESE	Total
	PRACTICAL							
11VL401	Project Work – Phase- II	0	0	24	12	100	100	200
				Total	**12**			

CA – Continuous Assessment, ESE – End Semester Examination

LIST OF ELECTIVES					
Course Code	**Course Title**	L	T	P	**C**
11VL011	DSP Processor Architecture and Programming	3	0	0	3
11VL012	Genetic Algorithms and their Applications	3	0	0	3
11VL013	Neural Networks and Applications	3	0	0	3
11VL014	Low Power VLSI Design	3	0	0	3
11VL015	Analog VLSI Design	3	0	0	3
11VL016	Design of Semiconductor Memories	3	0	0	3
11VL017	VLSI Technology	3	0	0	3
11VL018	Electronic Design Automation Tools	3	0	0	3
11VL019	Advanced Computer Architecture	3	0	0	3
11VL020	Wireless Embedded Systems	3	0	0	3
11VL021	Computer Aided Design of VLSI Circuits	3	0	0	3
11VL022	Optimization Techniques for VLSI Design	3	0	0	3
11AE015	Electromagnetic Interference and Compatibility in System Design	3	0	0	3
11VL023	System on Chip	3	0	0	3
11VL024	Embedded System Design	3	0	0	3

11VL101 APPLIED MATHEMATICS FOR ELECTRONIC ENGINEERS

(Common to VLSI Design, Communication System & Computer and Communication Engineering Branches)

3 1 0 4

Objective:

On completion of the course the students are expected

- To understand the numerical techniques of linear algebraic equations and solution of boundary value problem using Laplace Transforms.
- To know the properties and applications of Special functions.
- To understand the basic concepts and properties of random variables and queuing theory.

MODULE – I **15**

Numerical Methods: System of equations- Solution by Gauss Elimination, Gauss-Jordan and LU decomposition method- Jacobi, Gauss-Seidal iteration method- Eigen values of a matrix by Jacobi and Power method.

Wave Equation: Solution of initial and boundary value problems- Characteristics- D'Alembert's Solution - Laplace transform solutions for displacement in a long string - a long string under its weight - a bar with prescribed force on one end.

MODULE– II **15**

Bessel Functions : Bessel's equation - Bessel Functions- Series Representation of Bessel functions – Recurrence relations of Bessel functions – Generating function – Jacobi series – Orthogonal property for Bessel functions

Legendre Polynomials: Legendre's equation - Legendre polynomials -Rodrigue's formula - Recurrence relations- Generating functions – Orthogonal property for Legendre polynomials – Expansion of an arbitrary function in a series of Legendre polynomials.

MODULE–III **15**

Random Variables: One dimensional Random Variable - Moments and MGF – Binomial, Poisson, Geometrical, Normal Distributions- Two dimensional Random Variables – Marginal and Conditional Distributions – Covariance and Correlation Coefficient.

Queuing Theory: Single and Multiple server Markovian queueing models - Steady state system size probabilities – Little's formula – Priority queues – M/G/1 queueing system – P.K. formula.

Lecture: 45, Tutorial: 15, TOTAL: 60

REFERENCE BOOKS

1. Kapur, J.N. and Saxena, H.C., "Mathematical Statistics", S.Chand & Co., New Delhi, 2007.
2. Grewal, B.S. "Higher Engineering Mathematics", Khanna Publishers, New Delhi, 2007.
3. Sankara Rao, K. "Introduction to Partial Differential Equation", Prentice Hall of India, New Delhi, 1995.
4. Taha, H.A., "Operations Research- An Introduction", 6th Edition, Prentice Hall of India, New Delhi, Reprint 2010.
5. Jain, M.K., Iyengar, S.R.K. and Jain, R.K., "Numerical Methods for Scientific and Engineering Computation", New Age International (P) Ltd, Publishers, New Delhi, 2008.

11VL102 ADVANCED DIGITAL SYSTEM FOR IC DESIGN

3 1 0 4

Objective:

- To introduce the analysis and design of synchronous and asynchronous circuits.
- To introduce the algorithms for testing of digital circuits.
- To introduce the synchronous design using PLDs.

MODULE –I **15**

Sequential Circuit Design: Analysis of Clocked Synchronous Sequential Networks (CSSN)-Modeling of CSSN – State table Reduction- Stable Assignment – Complete Design of CSSN – Design of Iterative Circuits -Algorithmic State Machine (ASM)-ASM Chart – Synchronous Sequential Network Design Using ASM Charts- State Assignment- ASM Tables-ASM Realization-Asynchronous Inputs.

MODULE –II **15**

Asynchronous Circuit Design and Fault Diagnosis: Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC – State Assignment – Problem and the Transition Table – Design of ASC – Static and Dynamic Hazards – Essential Hazards – Data Synchronizers – Designing Vending Machine Controller – Mixed Operating Mode Asynchronous Circuits. - Fault Table Method – Path Sensitization Method – Boolean Difference Method – D Algorithm – Tolerance Techniques – The Compact Algorithm

MODULE–III **15**

Testability Algorithms and Programmable Devices: Practical PLA's – Fault in PLA – Test Generation – Masking Cycle – DFT Schemes – Built-in Self Test.Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a PAL – Realization State machine using PLD – Complex Programmable Logic Devices (CPLDs) – FPGA – Xilinx FPGA – Xilinx 3000 - Xilinx 4000

Lecture: 45, Tutorial: 15, TOTAL: 60

REFERENCE BOOKS

1. Givone Donald G., "Digital Principles and Design", Tata McGraw-Hill, New Delhi, 2002.
2. Biswas Nripendra N, "Logic Design Theory", Prentice Hall of India, New Delhi, 2001.
3. Yarbrough, John M., "Digital Logic Applications and Design", Thomson Learning, Singapore, 2001.
4. Roth Charles H., "Fundamentals of Logic Design", Thomson Learning, Singapore, 2005.
5. Ming-Bo Lin, "Digital System Design and Practices: Using Verilog HDL and FPGAs", Wiley Publisher, New York, 2008.

11VL103 VLSI DESIGN TECHNIQUES

3 0 0 3

Objective :

- To learn the MOS transistor theory
- To study the CMOS Fabrication Process.
- To Learn the CMOS circuit and logic design, Subsystem design.

MODULE – I **15**

Mos Transistor Theory: Introduction to I.C Technology- Basic MOS transistors- Threshold Voltage-Body effect.-Basic D.C. Equations-Second order effects- MOS models-Small signal A.C characteristics- The complementary CMOS inverter-DC characteristics-Static Load MOS inverters-The differential inverters- Transmission gate-CMOS processing technology **:**Silicon semiconductor technology-Wafer processing, Oxidation, epitaxy, deposition, Ion implantation. CMOS technology: nwell, pwell process. Silicon on insulator.

MODULE - II **15**

Circuit Characteristics and Performance Estimation: CMOS process enhancement-Interconnect and circuit elements-Stick diagram-Layout design rules. Latch up-Résistance estimation-Capacitance estimation-MOS capacitor characteristics-Device capacitances-Diffusion capacitance- SPICE modeling of MOS capacitance-Routing capacitance. Distributed RC effects-Inductance-Switching characteristics-Rise time, Fall time-Delay time- Empirical delay models- Gate delays- CMOS gate transistor Sizing -Power dissipation- Scaling of MOS transistor dimensions-CMOS Logic gate design-Fan in and fan out- Typical CMOS NAND and NOR delays- Transistor sizing.

MODULE-III **15**

CMOS Circuit and Logic Design: Different types of CMOS logic structures-Complementary logic-BICMOS logic- PseudonMOS logic- Dynamic CMOS logic- Clocked CMOS logic- Pass transistor logic- CMOS domino logic- NP domino logic- Cascade voltage switch logic- Source follower pull up Logic (SFPL)- Clocking strategies – I/O structures-Data path operations-Addition/subtraction-Parity generators-Comparators-Zero/one detectors-Binary Counters-ALUs-Multiplication: Array, Radix-n, Wallace Tree and Serial Multiplication- Shifters-Memory elements- RWM, Rom, Content Addressable Memory- Control: FSM, PLA Control Implementation.

TOTAL: 45

REFERENCE BOOKS

1. Weste, Neil.H.E. and Eshragian, K., “Principles of CMOS VLSI Design”, Second Edition, Addison-Wesley, New York, 2000.
2. Pucknell, Douglas A and Eshragian, K., “Basic VLSI Design”, Third Edition, Prentice Hall of India, New Delhi, 2000.
3. Baker, R. Jacob., LI, Harry W. and Boyce, David K., “CMOS Circuit Design”, Prentice Hall of India, New Delhi, 2000.
4. www.angelfire.com/electronic/in/vlsi/books.html
5. Hodges David A., Jackson Horace G., and Saleh Resve A., “Analysis and Design of Digital Integrated Circuits”, Third Edition, McGraw-Hill, New York, 2004.

11VL104 VLSI SIGNAL PROCESSING

(Common to M.E. VLSI Design, Applied Electronics, Control and Instrumentation Engineering)

3 1 0 4

Objective:

- To provide a comprehensive coverage of techniques for designing efficient DSP architectures.
- The architectural optimization both at block level as well as logic level are considered to realize architectures that can process high throughput data.
- To know the concepts of pipelined adaptive filters

MODULE – I **15**

Introduction to DSP Systems and Retiming: Introduction To DSP Systems -Typical DSP algorithms; Iteration Bound – data flow graph representations, loop bound and iteration bound, Algorithms For Computing Iteration Bound, Iteration Bound of Multirate Data Flow Graphs. Pipelining and parallel processing – Pipelining of FIR digital filters, parallel processing, pipelining and parallel processing for low power; Retiming - definitions and properties Retiming techniques; Solving systems of inequalities, Retiming Techniques.

MODULE– II **15**

Unfolding, Folding, Fast Convolution: Unfolding – an algorithm for Unfolding, properties of unfolding, Critical path Unfolding and Retiming applications of Unfolding- sample period reduction and parallel processing application; Folding – Folding transformation – Register minimizing techniques –Register minimization in folded architectures-Folding of Multirate systems. Fast convolution – Cook-Toom algorithm, modified Cook-Took algorithm – Wino grad Algorithm, Modified Wino grad Algorithm, Iterated Convolution – Cyclic Convolution-Design of Fast Convolution algorithm by inspection.;

MODULE-III **15**

Pipelined and Parallel Recursive and Adaptive Filters: Algorithmic strength reduction in Filters-Parallel FIR Filters, DCT and Inverse DCT, Parallel architectures for rank order Filters. Pipelined and parallel recursive and adaptive filters – inefficient/efficient single channel interleaving, Look- Ahead pipelining in first- order IIR filters, Look-Ahead pipelining with power-of-two decomposition parallel processing of IIR filters, combined pipelining and parallel processing of IIR filters, pipelined adaptive digital filters-relaxed look-ahead, pipelined LMS adaptive filter.

Lecture: 45, Tutorial: 15, TOTAL : 60

REFERENCE BOOKS

1. Parhi, Keshab K., "VLSI Digital Signal Processing Systems, Design and Implementation", John Wiley, Inter Science, New York, 1999.
2. Isamail, Mohammed and Fiez, Terri, "Analog VLSI Signal and Information Processing", McGraw-Hill, New York, 1994**.**
3. www.pdf-search-engine.com/vlsi-signal-processing-pdf.html
4. Magdy A. Bayoumi, Magdy A. Bayoumi, E. Swartzlander, "VLSI Signal Processing Technology", Kluwer Academic Publishers.October 1994
5. Ray Liu K J, "High Performance VLSI Signal Processing, Innovative architectures and Algorithms",IEEE Press,1998

11VL105 DEVICE MODELING

(Common to M.E. VLSI Design and Applied Electronics)

3 0 0 3

Objective:

- To introduce the properties of Semiconductor Devices
- To understand second order effects of Semiconductor Devices
- To understand how the properties of Semiconductor Devices are modeled and simulated

MODULE -I **15**

Semiconductor Physics and Diode Modeling: Quantum Mechanical Concepts- Carrier Concentration- Transport Equation- Mobility and Resistivity- Carrier diffusion- Carrier Generation and Recombination- Continuity equation- Tunneling and High field effects- Abrupt and linear graded PN junction- Ideal diode current equation- Static, Small signal and Large signal models of PN junction Diode-SPICE model for a Diode- Temperature and Area effects on Diode Model Parameters- Structure of Photo Conductors and PIN Photo Diode- Modeling of Photo Conductor- Structure of LASER- LASER rate equation - Static and dynamic modeling of LASER.

MODULE -II **15**

Bipolar Device Modeling and Parameter Measurements: Transistor Action-Terminal currents - Switching- Static, Small signal and Large signal Eber-Moll models of BJT- Gummel Poon Model- SPICE modeling - temperature and area effects- Bipolar Junction Transistor Static Parameter Measurement Techniques – Large signal parameter Measurement Techniques- Gummel Plots

MODULE- III **15**

MOSFET Modeling and Parameter Measurements: MOS Transistor – NMOS- PMOS – MOS Device equations - Threshold Voltage – Second order effects - Temperature Short Channel and Narrow Width Effect- Models for Enhancement- Depletion Type MOSFET- MOS Models in SPICE- MOSFET: Long and Short Channel Parameters and Measurement of Capacitance

TOTAL : 45

REFERENCE BOOKS

1. Massobrio Giuseppe and Antognetti Paolo, “Semiconductor Device Modeling with SPICE”, Second Edition, McGraw-Hill Inc, New York, 1993.
2. Sze S. M., “Semiconductor Devices-Physics and Technology”, 2nd Edition, John Wiley and Sons, New York, 2002.
3. Pallab Bhatacharya, “Semiconductor Opto-electronic Devices” 2nd Edition, Prentice Hall of India, New Delhi, 1996.
4. M.S. Tyagi, “Intorduction to Semiconductor Materials and Devices”, John Wiley, New York, 2003
5. Ben,G.Streetman, “Solid State Circuits”, 5th Edition, Prentice Hall of India, New Delhi, 2005.
6. De Graaf H.C and Klaasen F M.- “Compact Transistor Modeling for Circuit Design”, Springer-Verlag, New York,1990.

11VL106 HDL FOR IC DESIGN

3 0 0 3

Objective:

- To understand and learn the Hardware Description Language
- To enable the students to implement, practical digital functional blocks using HDL.
- To learn the concepts of RTL system design

MODULE – I **15**

VHDL For Digital System Design: VHDL Description of combinational Network-Modeling FF using VHDL process-VHDL model for a multiplexer-Compilation and Simulation of VHDl Code-Modeling a Sequential Machine-Variable,Signals and Constants-Arrays-VHDL Operators-VHDl functions –VHDL Procedures-Packages and Libraries.Design of a Serial Adder with accumulator, State Graph for a control network-Design of Binary Multiplier-Multiplication of signed binary number-Design of a binary divider-Binary decoder-Binary encoder-Multiplexer-Demultiplexer.

MODULE- II **15**

Modeling and Logic Synthesis with Verilog HDL: Overview of digital design using Verilog HDL-Hierarchical Modeling concepts-Basic Concepts-Gate level Modeling-Dataflow Modeling-Behaviour Modeling-Tasks and Functions-Switch level modeling. Verilog HDL Synthesis-Synthesis Design Flow-Verification of the gate level net list-Modeling for logic synthesis-Example of sequential circuit synthesis.

MODULE -III **15**

RTL System Design: RTL System-Execution Graph-Organization of system-Implementation of RTL System-Analysis of RTL System-Design of RTL System-Data Subsystem-Storage Modules-Functional Modules-Data path control subsystem-Micro programmed Controller-Microinstruction format-Microinstruction sequencing-Microinstruction Timing-Basic Components of a Micro Memory Subsystem. -Floating point Arithmetic-Representation of Floating point Number-Floating Point Multiplication

TOTAL : 45

REFERENCE BOOKS

1. Roth C.H., “Digital System Design using VHDL”, Thomson Learning, Singapore, 2001.
2. Navabi, “VHDL Analysis and Modeling of Digital Systems”, McGraw-Hill, New York..
3. Stephen Brown and Zvonko Vranesic, “Fundamentals of Digital Logic with VHDL Design”, Second Edition, McGraw-Hill, New York, 2005.
4. Samir Palnitkar, “Verilog HDL: A Guide to Digital Design and Synthesis”, Pearson Education, New Delhi, 2003.
5. Perry Douglas L., “VHDL: Programming by Example”, Fourth Edition, Tata McGraw-Hill, New Delhi, 2002.

11VL107 SIMULATION AND SYNTHESIS LABORATORY

0 0 4 2

LIST OF EXPERIMENTS

USING VHDL

1. Modeling of Sequential Digital Systems
2. Testbenches
3. State Machine Design
4. Memory Design
5. Design and implementation of ALU, MAC using FPGA
6. Design and implementation of different adders using FPGA
7. Design and implementation of Real time clock using FPGA
8. Design and implementation of 4 x 4 matrix keypad using FPGA
9. Design and implementation of UART using FPGA

SPICE MODELING (Microwind)

1. Simulation of NMOS circuits
2. Simulation of CMOS Circuits –Inverter, AND, OR
3. Simulation of CMOS Circuits –Half adder, full adder

11VL201 ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

3 0 0 3

Objective:

- To provide principles of analog integrated circuit analysis.
- To provide the design knowledge, which are required in analog IC design industry and research.
- To understand the analysis of operational amplifiers.

MODULE – I **15**

Models for Integrated Circuit Active Devices and Current Sources: Depletion region of a PN junction – large signal behavior of bipolar transistors- small signal model of bipolar transistor- large signal behavior of MOSFET- small signal model of the MOS transistors- short channel effects in MOS transistors – weak inversion in MOS transistors- substrate current flow in MOS transistor. MOS Current Mirrors – Simple, Cascode, Wilson and Widlar current source, Current sources.

MODULE - II **15**

Analog Design with MOS Technology and Linear ICs: Analysis of difference amplifiers with active load using BJT and FET, supply and temperature independent biasing techniques, voltage references. Output stages: Emitter follower, source follower and Push pull output stages. CMOS Class AB output stages – Two stage MOS Operational Amplifiers, with Cascode, MOS Telescopic-Cascode Operational Amplifier – MOS Folded Cascode and MOS Active Cascode Operational Amplifiers.

MODULE-III **15**

Operational Amplifiers and Analog Multipliers: Analysis of operational amplifiers circuit, slew rate model and high frequency analysis, Frequency response of integrated circuits: Single stage and multistage amplifiers, Operational amplifier noise. Analysis of four quadrant and variable trans conductance multiplier, voltage controlled oscillator, closed loop analysis of PLL, Monolithic PLL design in integrated circuits: Sources of noise- Noise models of Integrated-circuit Components – Circuit Noise Calculations – Equivalent Input Noise Generators – Noise Bandwidth – Noise Figure and Noise Temperature.

TOTAL : 45

REFERENCE BOOKS

1. Gray Paul R, Hurst Paul J and Lewis Stephen H, “Analysis and Design of Analog Integrated Circuits”, Fourth Edition, John Wiley & Sons, New York, 2002.
2. Franco Sergio, “Design with Operational Amplifiers and Analog Integrated Circuits”, Third Edition, McGraw-Hill, New York, 2001.
3. Das Gupta, Nandita and Dasgupta Amitava., “Semiconductor Devices, Modeling and Technology”, Prentice Hall of India, New Delhi, 2004.
4. David Johns and Ken Martin, “Analog Integrated Circuit Design”, John Wiley & Sons, New York, 1997
5. Paul R Gray, “Analysis and Design of Analog Integrated Circuits”, Fourth Edition, John Wiley & Sons, New York, 2002.

11VL202 APPLICATION SPECIFIC INTEGRATED CIRCUITS

3 0 0 3

Objective:

- To learn the different types of programmable ASIC,
- To study the concepts of interconnection and design tools.
- To study the concepts of VHDL and Verilog logic synthesis
- To know the details of floor planning, placement and routing.

MODULE - I **15**

Introduction to ASICs and Programmable ASICs: Types of ASICs - Design flow - CMOS transistors CMOS Design rules -Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors - Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture. Programmable ASICs: Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks- Actel ACT - Xilinx LCA –Altera FLEX.

MODULE - II **15**

Interconnects and Design Tools, Logic Synthesis: Altera MAX DC & AC inputs and outputs -Clock & Power inputs - Xilinx I/O blocks.Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC – Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.Logic Synthesis: Verilog and logic Synthesis-VHDL and logic Synthesis.

MODULE – III **15**

Simulation, Testing and Physical Design: Simulation and Testing: Types of simulation –boundary scan test - fault simulation - automatic test pattern generation.

System partition - FPGA partitioning - partitioning methods - floor planning -placement - physical design flow –global routing - detailed routing - special routing -circuit extraction - DRC.

TOTAL: 45

REFERENCE BOOKS

1. Smith, M.J.S., "Application Specific Integrated Circuits", Addison –Wesley, New York, 1997.
2. Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SOCs": A Practical Approach, Prentice Hall PTR, New Jersey, 2003.
3. Baskar, J., "VHDL Primer", McGraw-Hill, New York, 2005.
4. Wayne Wolf., "FPGA-Based System Design", Prentice Hall PTR, New Jersey,2004.
5. Razak Hossain, "High Performance ASIC Design: using Synthesizable Domino logic in an ASIC flow", Cambridge University Press,2008.

11VL203 TESTING OF VLSI CIRCUITS

3 0 0 3

Objective:

- To learn the concepts of VLSI testing of digital circuits,
- To design a design for testability, test pattern generation
- To learn logic level diagnosis and system level diagnosis

MODULE – I **15**

Introduction and Combinational Circuit Testing: Introduction to Testing - Faults in digital circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault location - Fault dominance - Logic Simulation - Types of simulation - Delay models - Gate level Event-driven simulation Test generation for combinational logic circuits - Testable combinational logic circuit design

MODULE – II **15**

Sequential Circuit Testing and Design for Testability: Test generation for sequential circuits - design of testable sequential circuits

Design for Testability - Ad-hoc design - Generic scan based design - Classical scan based design - System level DFT approaches

MODULE- III **15**

BIST and System Level Diagnosis: Built-In Self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test algorithms - Test generation for Embedded RAMs Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA – Test Generation -Micro processor and Microcontrollers testing – Register decoding - Instruction decoding - data storage, transfer, manipulation functions - Testing analog components. Testability features for board test. Design Verification

TOTAL :45

REFERENCE BOOKS

1. Abramovici, M., Breuer, M.A and Friedman, A.D., "Digital Systems and Testable Design", Jaico Publishing House, 2002.
2. Lala, P.K., "Digital Circuit Testing and Testability", Academic Press, 2002.
3. Bushnell, M.L and. Agrawal, V.D., "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwar Academic Publishers, 2002.
4. Nilcolici Nicoda, Al- HAshmini, " Power constrained Testing of VLSI Circuits", Kluwer Academic Publishers,2003.
5. Launs – Terng wang, Cheng – wen wu, Xidogingwen, " VLSI Testing Principles and Architectures: Design for Testability", Morgan Kaufmann Publisher,2006.

11VL204 DIGITAL SIGNAL PROCESSING INTEGRATED CIRCUITS

3 0 0 3

Objective:

- To understand the implementation of DSP concepts in VLSI architecture
- To know the concepts of accumulator and pipelining concepts
- To understand the concepts of redundant arithmetic and bit-level arithmetic architectures

MODULE – I **15**

Scaling ,Roundoff Noise and Lattice Structure: Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP
system design,; Scaling and Roundoff Noise- State variable Description of digital filters, Scaling and roundoff noise computation, Roundoff noise in pipelined IIR filters, Roundoff noise computation using State Variable description.Introduction, Schur algorithm, Digital basic Lattice Filters, Derivation of One-Multiplier Lattice Filter, Derivation of Normalized Lattice filter, Derivation of Scaled-Normalized Lattice Filter, Roundoff Noise Calculation in Lattice filters, Pipelining of Lattice IIR Digital Filters, Design Examples of Pipelined Lattice Filters, Low-Power CMOS Lattice IIR Filters.

MODULE - II **15**

Redundant Arithmetic and Bit-Level Arithmetic Architectures: Number system representations, Redundant Arithmetic-Carry-Free Radix-2 Addition And Subtraction, Hybrid Radix-4 Addition, Radix-2 Hybrid Redundant Multiplication Architectures, Data Format Conversion, Redundant to Non redundant Converter, Numerical Strength Reduction-Introduction, Sub expression Elimination, Multiple Constant Multiplication, Sub expression Sharing in Digital Filters, Additive and Multiplicative Number Splitting. Introduction, Parallel Multipliers, Interleaved Floor-Plan and Bit-Plane-Based Digital Filters, Bit-Serial Multipliers, Bit-Serial Filter Design and Implementation, Canonic Signed Digit Arithmetic, Distributed Arithmetic-Problems, Bit –Parallel and Bit-Serial Arithmetic

MODULE- III **15**

Accumulator and Pipelining Concepts: Basic Shift accumulator, Improved Shift accumulator.Pipelining Concepts-Introduction, Synchronous Pipelining and Clocking Styles, Clock Skew and Clock Distribution in Bit-Level Pipelined VLSI Designs, Wave Pipelining, Constraint Space Diagram and Degree of Wave Pipelining, Implementation of Wave-Pipelined Systems, Asynchrounous Pipelining, Signal Transition Graphs, Use of STG to Design Interconnection Circuits, Implementation of Computational Units, Problems. Layout of VLSI Circuits, DCT Processor as case studies.

TOTAL : 45

REFERENCE BOOKS

1. Parhi Keshab K.., " VLSI Digital Signal Processing Systems Design and Implementation" A Wiley-Interscience Publication, John Wiley & Sons,INC,1999.
2. Wanhammer, Lars., **"**DSP Integrated Circuits**"**, Academic press, New York, 1999.
3. Oppenheim, A.V and Schafer, Ronald W. "Discrete-Time Signal Processing", Pearson Education, 2000.
4. Ifeachor, Emmanuel C. and Jervis, Barrie W., **"**Digital Signal Processing – A Practical Approach**",** 2nd Edition, Pearson Education Asia, 2001.
5. Perelroyzen E., "Digital Integrated circuits: Design- for- Test using Simulink and State flow", CRC press, 2006.

11VL205 PROGRAMMABLE DEVICES LABORATORY

0 0 4 2

LIST OF EXPERIMENTS

USING VERILOG

10. Modeling of Sequential Digital Systems
11. Testbenches
12. State Machine Design
13. FIFO
14. Design and implementation of pipelined array multiplier using FPGA
15. Design and implementation of Traffic light controller using FPGA
16. Design and implementation of BOOTH Algorithm using FPGA
17. Design and implementation of 4 x 4 matrix keypad using FPGA
18. Implementation of various DSP algorithms

USING MICROWIND

4. Logic design using pass transistor and transmission gates
5. Multiplexer
6. Flipflops

11VL206 ASIC DESIGN LABORATORY

0 0 4 2

LIST OF EXPERIMENTS:

1. RTL verification
2. Checking functionality and timing Using standard cell library
3. I/O pad design
4. Standard cell designing
5. Floor planning
6. Placement
7. Routing
8. Analog circuits simulation
9. Layout design for analog circuits
10. Prime time-post timing analysis

11VL011 DSP PROCESSOR ARCHITECTURE AND PROGRAMMING

3 0 0 3

Objective:

- To understand the architectural features of various DSP processor
- To implement the DSP algorithms using the DSP Processor
- To learn the Blackfin processor

PREREQUISITE: Digital Signal Processing.

MODULE – I **15**

TMS320C54XX and TMS320C6X: Fundamentals of Programmable DSPs - Architecture of TMS320C54X-54X Buses-Memory organization-Computational Units-Pipeline operation-On-chip peripherals –Address Generation Units- Addressing modes and instruction set- assembly language instructions -Introduction to Code Composer studio- Architecture of TMS320C6X – Computational units-Addressing modes –Memory architecture- pipeline operation- instruction set- assembly language instructions

MODULE - II **15**

Blackfin Processor(BF537): Architecture of BF537- Computational units - Internal Memory organization- System interrupts – Direct Memory Access- on-chip peripherals-ALU-MAC-DAG Units-Addressing modes-Assembly language instructions- Timers –Interrupts-Serial ports-UART-Simple programs

MODULE- III **15**

Applications Using TMS320C54X/C6X/BF537: Program development - Software Development Tools- The Assembler and the Assembly Source File Filter design- Linker and Memory Allocation - DSP Software Development Steps- Speech Digitization-Encoding & Decoding-Image compression-Restoration-Adaptive Echo cancellation-Modulation

TOTAL: 45

REFERENCE BOOKS

1. Venkataramani, B. and Bhaskar, M., “Digital Signal Processors: Architecture, Programming and Applications”, Tata McGraw–Hill, New Delhi, 2003.
2. Texas Instrumentation, “User guides: Analog Devices”, Motorola Inc, Arizona, 2003.
3. Sen.M.Kuo, Woon–Seng S.Gan, “Digital Signal Processors: Architecture, Implementation and Applications”, Prentice Hall, 2005
4. www.analogdevices.com.
5. www.adi.com

11VL012 GENETIC ALGORITHMS AND THEIR APPLICATIONS

3 0 0 3

Objective:

- To learn the fundamentals of Genetic algorithm
- To implement the genetic algorithm concepts
- To learn the optimization techniques

PREREQUISITE: Neural Networks and Fuzzy Logic.

MODULE - I **15**

Fundamentals of Genetic Algorithm and Genetic Technology: Fundamentals of genetic algorithm: A brief history of evolutionary computation biological terminology-search space -encoding, reproduction-elements of genetic algorithm-genetic modeling-comparison of GA and traditional search methods.Genetic technology: steady state algorithm - fitness scaling - inversion. Genetic programming - Genetic Algorithm in problem solving.

MODULE - II **15**

Genetic Algorithm Implementation and Optimization: Genetic Algorithm in engineering and optimization-natural evolution –Simulated annealing and Tabu search .Genetic Algorithm in scientific models and theoretical foundations.Implementing a Genetic Algorithm – computer implementation - low level operator and knowledge based techniques in Genetic Algorithm**.**

MODULE-III **15**

Applications: Applications of Genetic based machine learning-Genetic Algorithm and parallel processors, composite laminates, constraint optimization, multilevel optimization, real life problem.

TOTAL: 45

REFERENCE BOOKS

1. Mitchell, Melanie., "An Introduction to Genetic Algorithm", Prentice-Hall of India, New Delhi, 2004.
2. Golberg, David.E., "Genetic Algorithms in Search, Optimization and Machine Learning", Addison Wesley, New York, 1999.
3. Nilsson, Nils.J., "Artificial Intelligence: A New Synthesis", Morgan Kauffmann Publishers Inc, San Francisco, 1998.
4. Rajasekaran, S. and Vijayalakshmi Pai, G.A., "Neural Networks, Fuzzy Logic and Genetic Algorithms, Synthesis and Applications", Prentice Hall of India, New Delhi, 2003.
5. Roger Jang, Chuen Tsai Sun and Eiji Mizutani, "Neuro Fuzzy and Soft Computing- A computational Approach for Learning and Machine Intelligence", Prentice Hall, 1996

11VL013 NEURAL NETWORKS AND APPLICATIONS

3 0 0 3

Objective:

- To understand and learn the basic neuron structures and the learning rules.
- To understand the various neural network architectures and their implementation for applications.
- To learn the concepts of self organizing maps

PREREQUISITE: Adaptive Networks

MODULE – I **15**

Learning Algorithms and Radial Basis Function Networks: Biological Neuron – Artificial Neural Model - Types of activation functions –Architecture: Feedforward and Feedback – Learning Process – Supervised and Unsupervised Learning – Learning Tasks - Statistical Learning Theory-– Single Layer Perceptron – Multilayer Perceptron – Back Propagation Algorithm – XOR problem – Limitations of Back Propagation Algorithm. Radial Basis Function Network: Exact Interpolator – Regularization Theory – Generalized Radial Basis Function Networks - Learning in Radial Basis Function Networks - Applications: XOR Problem –Image Classification.

MODULE - II **15**

Support Vector Machines and Attractor Neural Networks: Support Vector Machine:Optimal Hyper plane for Linearly Separable Patterns and Nonseparable Patterns – Support Vector Machine for Pattern Recognition – XOR Problem -insensitive Loss Function –Support Vector Machines for Nonlinear Regression. Associative Learning – Attractor Neural Network Associative Memory – Linear Associative Memory – Hopfield Network – Content Addressable Memory – Strange Attractors and Chaos - Error Performance of Hopfield Networks - Applications of Hopfield Networks – Simulated Annealing – Boltzmann Machine – Bidirectional Associative Memory – BAM Stability Analysis – Error Correction in BAMs – Memory Annihilation of Structured Maps in BAMS – Continuous BAMs – Adaptive BAMs – Applications.

MODULE - III **15**

Adaptive Resonance Theory and Self Organising Maps: ART Networks:Noise-Saturation Dilemma - Solving Noise-Saturation Dilemma – Recurrent On-center –Off-surround Networks – Building Blocks of Adaptive Resonance – Substrate of Resonance Structural Details of Resonance Model – Adaptive Resonance Theory –Applications. Self-organizing Map – Maximal Eigenvector Filtering – Sanger's Rule – Generalized Learning Law – Competitive Learning - Vector Quantization – Mexican Hat Networks - Self-organizing Feature Maps – Applications.

TOTAL : 45

REFERENCE BOOKS

1. Haykin Simon., "Neural Networks: A Comprehensive Foundation", Second Edition, Addison Wesley, New York, 2001.
2. Satish Kumar, "Neural Networks: A Classroom Approach", Tata McGraw-Hill, New Delhi, 2004.
3. Martin T. Hagan, Howard B. Demuth, Mark H. Beale, "Neural Network Design", PWS Pub Company, 1995.
4. Laurene V. Fausett "Fundamentals of Neural Network: Architectures Algorithms and Applications" Prentice Hall, 1993
5. Danilo P. Mandic , Jonathon A., "Recurrent Neural Networks for Prediction: Learning Algorithms, Architectures and Stability", John Wiley and Sons, 2001

11VL014 LOW POWER VLSI DESIGN

(Common to M.E. Applied Electronics and VLSI Design)

3 0 0 3

Objective:

- To understand the concepts of power dissipation and power optimization in CMOS circuits.
- To learn the concepts of designing low power CMOS circuits
- To study the concepts of software design for low power

PREREQUISITE: VLSI Design Techniques.

MODULE – I **15**

Power Dissipation and Power Optimization in CMOS: Hierarchy of limits of power: Fundamental Limit, Material Limit, Device Limit,Circuit Limit, System Limit and Practical Limit – Sources of power consumption –Physics of power dissipation in CMOS FET devices: MIS Structure, Long channel andSubmicron MOSFET- Basic principle of low power design.Power optimization: Logical level power optimization: Combinational circuits technology, Sequential circuits technology, Technology dependent optimization.Circuit level low power design: Introduction, Latches and FlipFlops, Transistor sizing and Ordering.

MODULE- II **15**

Design of Low Power CMOS Circuits and Power Estimation: Circuit techniques for reducing power consumption in adders and multipliers- Logic stylesComputer Arithmetic techniques for low power systems: LNS, RNS. Reducing powerconsumption in memories: SRAM, DRAM. Low power clock, Interconnect and layout design. Power estimation techniques: Logic level power estimation: Simulation power analysis: Monte Carlo Power Estimation, Advanced Sampling Techniques and Vector Compaction. Probabilistic power analysis: Combinational Circuits, Real Gate delay power Estimation, Sequential circuits.

MODULE-III **15**

Synthesis and Software Design for Low Power: Synthesis for low power: Behavioral level transforms: Algorithm Level Transforms forlow power, Architecture driven voltage scaling, PCLS optimization for Adaptive andNon adaptive filters. Power optimization using operation reduction, substitution.Software design for low power: Sources of power dissipation, Software power optimization, Automated low power code generation, codesign for low power.Advanced techniques: Adiabatic computation, Pass Transistor Logic Synthesis,Asynchronous Circuits. Special techniques: Power reduction in clock networks, LowPower Swing bus, Delay balancing.

TOTAL: 45

REFERENCE BOOKS

1. Soudris, Dimitrios, Pignet, Chirstian, and Goutis, Costas., “Designing CMOS Circuits for Low Power”, Kluwer Academic Publishers, Dordrecht, 2002.
2. Yeap, Gary., “Practical Low Power Digital VLSI Design”, Kluwer Academic Publihsers, Dordrecht, 1998
3. Roy, K. and Prasad, S.C., “Low Power CMOS VLSI Circuit Design”, John Wiley, New York, 2000.
4. Chandrakasan, A.P., and Broadersen, R.W, “Low Power Digital CMOS VLSI Design”, Kluwer Academic Publishers, Dordrecht, 1995.
5. G.K Yeap and F. N Najm, “Low Power VLSI Design and Technology”, Springer, 1997.
6. Iman. Sasan, Pedlum Klassard, “Logic Synthesis for Low Power VLSI Design”, Springer. Kluwer Academic Publishers, 1997.

11VL015 ANALOG VLSI DESIGN

3 0 0 3

Objective:

- To learn the Mixed signal design concepts of CMOS, BICMOS circuits
- To understand the Analog VLSI interconnects.
- To learn and understand the Statistical modeling and simulation concepts.

PREREQUISITE: VLSI Design Techniques.

MODULE– I **15**

Basic CMOS And BICMOS Circuits: Mixed-Signal VLSI Chips-Basic CMOS Circuits-Basic Gain Stage-Gain Boosting Techniques-Super MOSTransistor- Primitive Analog Cells-Linear Voltage-Current Converters-MOS Multipliers and Resistors-CMOS,Bipolar and Low-Voltage BiCMOS Op-Amp Design-Instrumentation Amplifier Design-Low Voltage Filters.Continuous-Time Signal Processing-Sampled-Data Signal Processing-Switched-Current Data Converters-Practical Considerations in SI Circuits Biologically-Inspired Neural Networks - Floating - Gate, Low-Power Neural Networks-CMOS Technology and Models-Design Methodology-Networks-Contrast Sensitive Silicon Retina.

MODULE - II **15**

Sampled-Data Analog Circuits and Analog VLSI Interconnects: First-order and Second SC Circuits-Bilinear Transformation - Cascade Design-Switched-Capacitor Ladder Filter-Synthesis of Switched-Current Filter- Nyquist rate A/D Converters-Modulators for Over sampled A/D Conversion-First and Second Order and Multibit Sigma-Delta Modulators-Interpolative Modulators –Cascaded Architecture-Decimation Filters-mechanical, Thermal, Humidity and Magnetic Sensors-Sensor Interfaces. Analog Test Buses-Design for Electron -Beam Testablity- Physicsof Interconnects in VLSI-Scaling of Interconnects-A Model for Estimating Wiring Density-A Configurable Architecture for Prototyping Analog Circuits.

MODULE–III **15**

Statistical Modeling and Analog and Mixed analog-Digital Layout: Review of Statistical Concepts - Statistical Device Modeling- Statistical Circuit Simulation-Automation Analog Circuit Design-automatic Analog Layout-CMOS Transistor Layout-Resistor Layout-Capacitor Layout-Analog Cell Layout-Mixed Analog -Digital Layout.

TOTAL : 45

REFERENCE BOOKS

1. Ismail, Mohammed., Fiez, Terri., "Analog VLSI Signal and Information Processing", McGraw-Hill, New York, 1994.
2. Haskard, Malcom R., May, Lan C., "Analog VLSI Design - NMOS and CMOS", Prentice Hall, New Jersey, 1998.
3. Geiger, Randall L, and Allen, Phillip E., Strader, Noel K., “VLSI Design Techniques for Analog and Digital Circuits”, McGraw-Hill, New York, 1990.
4. France, Jose E., and Tsividis, Yannis., "Design of Analog Digital VLSI Circuits for Telecommunication and signal Processing", Prentice Hall, New Jersey, 1994.
5. Ballcir Sina, Dundar Gunhan, Ogrenci Selcuk, “Analog VLSI Design Over Guide”, CRC Press, 2008.

11VL016 DESIGN OF SEMICONDUCTOR MEMORIES

3 0 0 3

Objective:

- To learn memory cell structures and fabrication technologies.
- To know the application-specific memories and architectures.
- To study the concepts of memory design, fault modeling and test algorithms, limitations, and trade-offs.
- To understand memory stacks and multichip modules for gigabyte storage.

PREREQUISITE: VLSI Design Techniques, ASIC Design

MODULE– I **15**

Random Access Memories , Fault Modeling, Testing and Reliability: SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies-Silicon On Insulator (SOl) Technology-Advanced SRAM Architectures and Technologies-Application Specific SRAMs, DRAM Technology Development-CMOS DRAMs-DRAMs Cell Theory and Advanced Cell Strucutures-BiCMOS,DRAMs-Soft Error Failures in DRAMs- Advanced DRAM Designs and Architecture-Application Specific DRAMs, RAM Fault Modeling, Electrical Testing, Peusdo Random Testing-Megabit DRAM Testing General Reliability Issues-RAM Failure Modes and Mechanism

MODULE - II **15**

Nonvolatile Memories, Faulty Modeling and Testing: Masked Read-Only Memories (ROMs)-High Density ROMs-Programmable Read-Only Memories (PROMs)-Bipolar Proms-CMOS PROMs-Erasable (UV) -Programmable Road-Only Memories (EPROMs)-Floating-Gate EPROM Cell-One-Time Programmable (OTP) EPROMS-Electrically Erasable PROMs (EEPROMs)-EEPROM Technology And Architecture-Nonvolatile SRAM-Flash Memories(EPROMs or EEPROM)-Advanced Flash Memory Architecture, Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing-Application Specific Memory Testing, Nonvolatile Memory Reliability-Reliability Modeling and Failure Rate Prediction

MODULE-III **15**

Packaging Technologies and Reliability: Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques-Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics-Radiation Hardness Assurance and Testing - Radiation Dosimetry-Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog Memories-Magnetoresistive Random Access Memories (MRAMs)-Experimental Memory Devices. Memory Hybrids and MCMs (2D)-Memory Stacks and MCMs (3D)-Memory MCM Testing and reliability Issues-Memory Cards-High Density Memory Packaging Future Directions. Design for Reliability- Reliability Test Structures-Reliability Screening and Qualification.

TOTAL : 45

REFERENCE BOOKS

1. Sharma, Ashok K., “Semiconductor Memories: Technology, Testing, and Reliability”, Wiley-IEEE Press, New York, 2002.
2. http://www.siliconfareast.com
3. Smith, M.J.S., "Application Specific Integrated Circuits”, Addison –Wesley, New York, 1997
4. William D.Brown, Joe Brewer, Nonvolatile Semiconductor Memory Technology: A Comprehensive Guide to Understanding and Using NVSM Devices ,Wiley-IEEE Press 1997
5. Ashok K. Sharma , “Semiconductor Memories: Technology, Testing, and Reliability”, Wiley-IEEE Press 2002.

11VL017 VLSI TECHNOLOGY

3 0 0 3

Objective:

- To learn the concepts of silicon wafer preparation techniques.
- To study the concepts of lithography, Etching techniques
- To learn the process of deposition diffusion and ion implantation.
- To know the assembly techniques and packaging of VLSI devices.

PREREQUISITE: Device Modeling**.**

MODULE – I **15**

Crystal Growth, Wafer Preparation, Epitaxy, Oxidation and Lithography: Electronic Grade Silicon, Czochralski crystal growing, Silicon shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators,Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface,Oxidation of Poly Silicon, Oxidation inducted Defects Lithography: Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography.

MODULE- II **15**

Relative Plasma Etching, Deposition, Diffusion, Ion Implantation, Metalisation and Process Simulation: Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism –Measurement techniques - Range theory- Implant equipment.Annealing Shallow junction – High energy implantation – Physical vapour deposition – Patterning. Process Simulation: Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition.

MODULE-III **15**

Analytical, Assembly Techniques and Packaging of VLSI Devices: VLSI process integration**:** NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.

Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – banking design consideration – VLSI assembly technology – Package fabrication technology.

TOTAL: 45

REFERENCE BOOKS

1. Sze, S.M., "VLSI Technology", Second Edition, McGraw-Hill, New York, 1998.
2. Mukherjee, Amar., "Introduction to NMOS and CMOS VLSI System Design", Prentice Hall India, New Delhi, 2000.
3. Plummer, James D., Deal, Michael D. and Griffin, Peter B., "Silicon VLSI Technology: Fundamentals Practice and Modeling", Prentice Hall India, New Delhi, 2000.
4. Chen, Wai Kai., "VLSI Technology", CRC Press, London, 2003.
5. Yurii V Gulyaev and Yu L Kopylov, "VLSI technology: Fundamentals and Applications", 1988 Sov. Phys. Usp.

11VL018 ELECTRONIC DESIGN AUTOMATION TOOLS

3 0 0 3

Objectives:

- To learn the Synthesis and Simulation tools for digital circuits
- To understand the design of mixed signal circuit modeling
- To learn system design using system C

PREREQUISITE: HDL Languages.

MODULE - I **15**

Script Language and Synopsys: An overview of OS commands. System settings and configuration. Introduction to Unix commands. Writing Shell scripts. VLSI design automation tools. An overview of the features of practical CAD tools. Mixed signal circuit modeling and analysis using VHDL –AMS,-synopsys

MODULE - II **15**

Synthesis and Simulation: Synthesis and simulation using HDLs-Logic synthesis using verilog and VHDL. Memory and FSM synthesis. Performance driven synthesis, Simulation- Types of simulation. Static timing analysis. Formal verification. Switch level and transistor level simulation.

Circuit simulation - circuit description. AC, DC and transient analysis. Advanced spice commands and analysis. Models for diodes, transistors and opamp. Digital building blocks. A/D, D/A and sample and hold circuits. Design and analysis of mixed signal circuits.

MODULE – III **15**

System Design: System design using systemC- System C models of computation. Classical hardware modeling in system C. Functional modeling. Parametrized modules and channels. Test benches. Tracing and debugging.

TOTAL :45

REFERENCE BOOKS

1. M.J.S.Smith, Application Specific Integrated Circuits,Pearson,2002
2. M.H.Rashid, Spice for Circuits and Electronics using Pspice. (2/e), PHI.
3. T. Grdtker et al , System Design with SystemC, Kluwer, 2004.
4. P.J. Ashenden et al , The System Designer’s Guide to VHDL-AMS, Elsevier, 2005
5. www.semiconductorsimulation.com

11VL019 ADVANCED COMPUTER ARCHITECTURE

3 0 0 3

Objective:

- To introduce the Parallel processing and vector processors
- To know about the Multiprocessors
- To understand the Multicore Processors

PREREQUISITE: Computer Architecture

MODULE - I **15**

Principles of Parallel Processing and Vector Processors: Introduction-Trends towards Parallel Processing- Uniprocessor Architecture Overview–Basic Uniprocessor Architecture, Parallel Processing Mechanism, Balancing of subsystems, Bandwidth, Multiprogramming and Time sharing – Styles of Architecture -Multiplicity of Instruction – Data Structures, Serial versus Parallel Processing- Parallelism versus Pipelining- Parallel Processing Applications. Principles of Vector Processing, Pipelined Vector Processing methods, The Architecture of CRAY-1,the Architecture of CYBER-205, Vector Processing in CYBER-205.

MODULE - II **15**

Array Processors and Multiprocessor Systems: SIMD Computer Organizations, Masking and Data Routing mechanisms, Statics versus Dynamic Networks, Mesh-connected, Iliac Networks, Cube Interconnection Networks, SIMD Matrix Multiplication. Loosely Coupled Multiprocessors, Tightly Coupled Multiprocessors, Processor characteristics for Multiprocessing, Time Shared or Common Buses, Crossbar switch and Multi-port memories, Classification of Multiprocessor Operating Systems, Software Requirements for Multiprocessors, Operating System Requirements.

MODULE - III **15**

Data Flow Computer Architectures and Multi Core Processors: Control-Flow versus Data Flow Computers, Data Flow Graphs and LanguagesAdvantages and Potential Problems, Static Data Flow Computers, Dynamic Data FlowComputers, Data Flow Design Alternates - Introduction to Multi core processor – Components of multi core processors.-Applications

TOTAL: 45

REFERENCE BOOKS

1 Hwang, Kai, and Briggs, Faye A., "Computer Architecture and Parallel Processing," McGraw Hill Inc., New York, 1985.
2 Shiva, Sajjan G., "Pipelined and Parallel Computer Architecture", Prentice Hall Inc, New Jersey, 1996.
3 Stallings, William. "Computer Organization and Architecture", McMillan Publishing Company, London, 1990.
4 Hwang, Kai., "Advanced Computer Architecture", Tata McGraw-Hill, New Delhi, 2001.
5 www.intel.com/technology/advanced_comm/multicore.htm

11VL020 WIRELESS EMBEDDED SYSTEMS

3 0 0 3

Objective:

- To study the basic concepts of embedded system and its use in real time system.
- To study the protocol architectures of different wireless networks and its application in embedded systems.
- To learn the recent trends in sensor technologies

PREREQUISITE: Wireless Networks.

MODULE - I **15**

Wireless Embedded Systems for Real-Time Applications: Introduction - Definition of embedded system -Constraints on embedded systems vs.standalone systems- Concept of real-time design -Time scales for real-time system –Applications Software environments: HLL vs. assembly coding, DSP vs. general purpose computer vs. RISC.

Wireless PAN: Blue tooth:Over all architecture, Protocol Stack, Physical Connection, MAC Mechanism, Connection Management, Security-Zigbee: Protocol Architecture, Physical layer, MAC Layer,Zigbee Layer,Applications-Home RF_Wi Fi.

MODULE - II **15**

CDMA, GSM ,GPRS and Smart Sensors: IS-95:Forward CDMA Channel,Reverse CDMA Channel-GSM:Services,System Architecture, Radio Sub system,Channel Types,Frame structure,Signal Processing- GPRS-Reference Architecture, Protocol Layers,Short Messaging Services. Primary sensors, filters, converter – compensation – Non-linearity- Noise and interference – Drift – Information coding – Data coding – Data Communication

MODULE -III **15**

Recent Trends in Sensor Technologies and Applications: Standards for smart sensor interface – Film sensors – Semiconductor IC technology –MEMS – Nano sensors. Product,Bands and Standards-Wireless Geo location: System Architecture,Technologies, Standard for E-911 Service- Wireless Home Networking-Need,Technologies- Home Access Networks-Embedded Wireless Control using GSM-RFID.

TOTAL: 45

REFERENCE BOOKS

1. Iyer S. V. and Gupta P., “Embedded Real-time System Programming”, Tata McGraw-Hill, New Delhi, 2006.
2. Pahalavan, Kaveh and Krishnamoorthy, Prasanth., “Principles of Wireless Networks”, Prentice Hall of India, New Delhi, 2005.
3. Rappaport, Theodore S., “Wireless Communications: Principles and Practice”, Prentice Hall of India, New Delhi, 2007.
4. Patranabis, D., “Sensors and Transducers”, Wheeler Publishing, Allahabad, 1997.
5. Michel Banatre, Pedro Jose Marron, Anibal Ollero, “Cooperating Embedded Systems And Wireless Sensor Networks”, John Wiley & Sons Inc, 2008.

11VL021 COMPUTER AIDED DESIGN OF VLSI CIRCUITS

3 0 0 3

Objectives:

- To know the concepts of Physical design flow of VLSI circuits
- To study various algorithms used to automate the IC design process
- To understand the various steps involved in the design and fabrication of VLSI chips
- Emphasizes the Physical design automation of VLSI Design

PREREQUISITE:ASIC Design

MODULE - I **15**

Design Methodologies: Introduction to VLSI Design methodologies - Review of VLSI Design automation tools -Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable problems - general purpose methods for combinatorial optimization problems.

MODULE - II **15**

Layout Design: Layout Compaction - Design rules – problem formulation - algorithms for constraint graph compaction - Placement and Partitioning - Circuit representation – Placement algorithms – partitioning- Floor planning concepts - shape functions and floor plan sizing - Types of local routing problems - Area routing - channel routing - global routing - algorithms for global routing

MODULE-III **15**

Simulation and Synthesis: Simulation - Gate-level modeling and simulation - Switch-level modeling and simulation Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis. High level Synthesis - Hardware models - Internal representation - Allocation assignment and scheduling - Simple scheduling algorithm - Assignment problem – High level transformations

TOTAL: 45

REFERENCE BOOKS

1. Gerez, S.H., "Algorithms for VLSI Design Automation", John Wiley & Sons, New York, 2002.
2. Sherwani, N.A., "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, Boston, 2002
3. Hill, D., Shugard, D., Fishburn, J. and Keutzer, K., “Algorithms and Techniques for VLSI Layout Synthesis”, Kluwer Academic Publishers, Boston, 1989.
4. Drechsler, R., “Evolutionary Algorithms for VLSI CAD”, Kluwer Academic Publishers, Boston, 1998.
5. Sarafzadeh, C.K. Wong, “An Introduction to VLSI Physical Design”, Mc Graw Hill International Edition 1995

11VL022 OPTIMIZATION TECHNIQUES FOR VLSI DESIGN

3 0 0 3

Objectives:

- To understand the techniques of optimization problem.
- To develop the concept of Linear and Non-linear programming problems and finding solutions through various methods
- To know the types of functions and relations and their applications.
- To understand the basic concepts and properties of queuing theory and Constructing models to handle the complicated problems.

PREREQUISITE: Advanced Mathematics.

MODULE – I **15**

Linear Programming Problem: Mathematical Formulation – Basic definitions – Solutions of LPP: Graphical method, Simplex method –Big–M method and Two phase method – Duality theory – Dual simplex method.

Transportation Model: Mathematical Formulation – Methods for finding Initial Basic Feasible Solution – MODI method – Degeneracy in transportation problem – Unbalanced transportation problems – Maximization case in transportation problem.

MODULE –II **15**

Assignment Model :Mathematical Formulation – Hungarian algorithm – Unbalanced assignment problem – Maximization case in assignment model

Non-Linear Programming: Formulation of non–linear programming problem – Constrained optimization with equality constraints – Constrained optimization with inequality constraints – Graphical method of non–linear programming problem involving only two variables – Kuhn-tucker conditions with non-negative constraints.

MODULE–III **15**

Replacement Model: Introduction - Replacement of Items that Deteriorate – Replacement of Items that Fail Suddenly – Group Replacement policy.

Dynamic programming: Principle of optimality – Recursive equation approach – Application to shortest route, Cargo-loading, Allocation and Production schedule problems.

TOTAL : 45

REFERENCE BOOKS

1. Kanti Swarup Gupta, P.K and Man Mohan “Operations Research”, S.Chand & Co., 1997.
2. Trembly J.P and Manohar R, “Discrete Mathematical Structures with Applications to Computer Science”, Tata McGraw–Hill, New Delhi, 2008.
3. Kapur, J.N. and Saxena, H.C., “Mathematical Statistics”, S.Chand & Co., New Delhi, 2007.
4. Taha, H.A., “Operations Research- An Introduction”, 6th Edition, Prentice Hall of India, 2008.
5. www.elsevierdirect.com

11AE015 ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY IN SYSTEM DESIGN

(Common to M.E. Applied Electronics, VLSI Design, Communication Systems)

3 0 0 3

PREREQUISITES

Electromagnetic Theory, Circuit Theory

Objective:

- To give basics of Electromagnetic interference
- To introduce the concept of EMI coupling principles
- To impart the knowledge of EMI/EMC standards and measurements
- To design control circuits based on EMI
- To develop the EMC design of PCBs

MODULE- I **15**

EMI Environment: EMI/EMC concepts and definitions, Sources of EMI, conducted and radiated EMI, Transient EMI, Time domain Vs Frequency domain EMI, Units of measurement parameters, Emission and immunity concepts, ESD.

EMI Coupling Principles: Conducted, Radiated and Transient Coupling, Common Impedance Ground Coupling

MODULE- II **15**

EMI Coupling Principles: Radiated Common Mode and Ground Loop Coupling, Radiated Differential Mode Coupling, Near Field Cable to Cable Coupling, Power Mains and Power Supply coupling.

EMI/EMC Standards and Measurements: Civilian standards - FCC,CISPR,IEC,EN,Military standards - MIL STD 461D/462, EMI Test Instruments /Systems, EMI Shielded Chamber, Open Area Test Site, TEM Cell, Sensors/Injectors/Couplers, Test beds for ESD and EFT, Military Test Method and Procedures (462).

MODULE- III **15**

EMI Control Techniques: Shielding, Filtering, Grounding, Bonding, Isolation Transformer, Transient Suppressors, Cable Routing, Signal Control, Component Selection and Mounting

EMC Design of PCBs: PCB Traces Cross Talk, Impedance Control, Power Distribution Decoupling, Zoning, Motherboard Designs and Propagation Delay Performance Models.

TOTAL: 45

REFERENCE BOOKS

1. Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", Second Edition, John Wiley & Sons, New York, 1988.
2. Kodali, V.P., "Engineering EMC Principles, Measurements and Technologies", IEEE Press, London, 1996.
3. Keiser, Bernhard., "Principles of Electromagnetic Compatibility", Third Edition, Artech House, Dedham, 1986
4. Paul, C.R., "Introduction to Electromagnetic Compatibility", Second Edition, John Wiley & Sons, New York, 2006.
5. Kodali. Prasad., "Engineering Electromagnetic Compatibility: Principles, Measurements, Technologies and computer models", Second Edition, John Wiley & Sons, New York, 2001.

11VL023 SYSTEM ON CHIP

3 0 0 3

Objectives:

- To learn combinational system on chip design
- To learn the sequential system on chip design
- To understand the design of subsystem and cad systems

PREREQUISITE: VLSI Design Techniques.

MODULE- I **15**

Digital Systems: Digital system and VLSI-Transistors-Design rules-Layout design and tools-logic gates-static complementary gates-switch logic-alternative gate circuits-delay through resistive interconnect-delay through inductive interconnect

MODULE– II **15**

Combinational and Sequential Network: Combinational logic network-standard cell based layout-Combinational network delay-logic and interconnect design-power optimization-switch logic network-combinational logic testing Sequential machines-Latches and Flipflops-Sequential systems and clocking disciplines-Sequential System Design- Power optimization-Design Validation-Sequential testing

MODULE - III **15**

Subsystem Design: Subsystem Design-Principles of Shifters-Adders-ALU-Multiplier-High Density Memory-FPGA-PLA- Floor planning methods- off chip connections-Architectural Design –HDL-Register Transfer Design-High Level Synthesis-Architecture for low power-SoC and embedded CPUs-Architecture testing.- Chip Design-methodologies-Kitchen Timer Chip-Microprocessor Data Path CAD systems and algorithms-Switch level simulation-layout synthesis-analysis-timing analysis and optimization-logic synthesis-test generation-Sequential machine optimization-scheduling and binding- Hardware/Software co design

TOTAL :45

REFERENCE BOOKS

1. Wolf, Wayne "Modern VLSI Design: System-on-Chip Design", 3rd edition, Pearson Edition, New Delhi, 2004.
2. Reis, Ricardo., "Design of System on a Chip: Devices and Components", Springer, 2004.
3. Rashinkar P., Paterson and Singh L., "System on a Chip Verification – Methodologies and Techniques", Kluwer Academic Publishers, 2001.
4. Wang, Laung – Terng, Stroud, Charles.E., Touba, Nur.A, "System–on–Chip Test Architectures: Nanometer Design for Testability", Elsevier Inc,2007.
5. www.elsevier.com

11VL024 EMBEDDED SYSTEM DESIGN

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Objective:

- To give sufficient background of programming concepts and embedded programming in C and C++
- To understand the real time operating system concepts.
- To learn the interfacing concepts

PREREQUISITE: Microprocessor and Microcontroller.

MODULE - I **15**

Introduction to Embedded Processors: Introduction to Embedded Computing, Hardware Architecture-Software Architecture, Trends: SoC, custom designed chips, configurable processors and multi-core processors. Memory model – hierarchy and management, virtual memory concepts, protection and cache. Embedded Processors: General concepts – Instruction Set Architecture, Levels in architecture, Functional description – hardware/software trade-off Introduction to RISC architecture, pipelining, Instruction issue and execution, Instruction formats, Addressing modes, Data alignment and byte ordering, Introduction to Power PC Architecture.

MODULE- II **15**

Embedded Programming: Embedded System Software: Components of an embedded software system, system boot up and downloading code, System memory map (allocating sections through linker command file), Programming peripherals and ISRs, Embedded tool chain, Mixing C and Assembly- concurrent software- memory management and system initialization. Introduction to CodeWarrior development system.

MODULE- III **15**

Real-Time Operating System Concepts and Case Studies: Architecture of the Kernel-task and task scheduler-Interrupt Service Routines-Semaphores-Mutex-Mailboxes-Message Queues-Event Registers-Pipes-Signals-Timers-Memory Management – Priority Inversion Problem, Scheduling approaches, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems. Use of µC/OS-II- Case study of an Embedded system in Smart Card. Porting and running µC/OS-II in Cold Fire Processor for smart card applications.

TOTAL: 45

REFERENCE BOOKS

1. Furber Steve, "ARM System-on-chip Architecture", Second Edition, Pearson Education Ltd, New Delhi, 2000**.**
2. Vahid Frank and Givargis Tony**. "**Embedded System Design: A Unified Hardware/Software Introduction", John Wiley &sons, New York, 2002.
3. Raj Kamal., "Embedded Systems Architecture, Programming and Design", Tata McGraw-Hill, New Delhi, 2003.
4. Wolf Wayne.*,* "Computers as Components: Principles of Embedded Computing System Design", Morgan Kaufman Publishers, San Francisco, 2001.
5. Labrosse, Jean J., "Micro C/OS-II: The Real-Time Kernel", Second Edition, CMP Books Group west Publications, 2002.